IT IS CLAIMED:

1. In a system including a host and a plurality of sockets in which electronic circuit cards are mechanically insertable and electrically connectable, a method of operating the system, comprising:

transferring data between the host and a card addressed over a command circuit when connected to all of the plurality of sockets through a data circuit also connected to all of the plurality of sockets, and

normally transferring commands that control operation of the electronic circuit cards from the host to an individual card over the command circuit when connected to all of the plurality of sockets except when unique addresses of the individual cards are being defined by communication between the host and the cards one at a time over the command circuit that is alternatively connected to one of the plurality of sockets at a time.

2. The method of claim 1, further comprising:

storing within at least some of the electronic circuit cards a characteristic of a number of data contacts thereof through which data are transferrable in parallel,

causing the host to read the stored characteristic from each of the cards inserted into the plurality of sockets, and

wherein transferring data between the host and an addressed card includes transferring data over one or more of a plurality of data lines connecting the host with each of the plurality of sockets according to the characteristic stored in the addressed card.

3. The method of claim 2, wherein the host provides a clock signal to each of the plurality of sockets to operate electronic circuit cards inserted therein with a common clock frequency regardless of the number of lines over which

data are simultaneously transferred with the individual cards that are inserted into the sockets.

4. The method of any one of claims 1-3, wherein the electronic circuit cards include re-writeable non-volatile memory in which the transferred data are stored.

5. In a system including a host and at least one socket in which at least one of a plurality of electronic circuit cards is removably insertable at one time to form an electrical connection with contacts of the card, a method of operating the system, comprising:

storing within the individual electronic circuit cards a characteristic of a number of data contacts thereof through which data are transferrable in parallel,

causing the host to read the stored characteristic from said at least one card inserted into said at least one socket, and

transferring data between the host and said at least one inserted card over one or more of a plurality of lines connecting the host with said at least one socket according to the characteristic stored in the individual one inserted card.

6. The method of claim 5, wherein the host provides a clock signal to said at least one plurality of sockets to operate one inserted card with a common clock frequency regardless of the number of lines over which data are simultaneously transferred therewith.

7. The method of either one of claims 5 or 6, wherein the electronic circuit cards include re-writeable non-volatile memory in which the transferred data are stored.

8. The method of claim 7, wherein the host determines whether said one inserted card is a MMC type, and, if so, transfers data over only one of the plurality of data lines to said at least one socket.

9. The method of claim 7, wherein transferring data between the host and said at least one inserted card includes directing individual bits of a serial data stream in sequence through a number of said data lines corresponding to the characteristic stored in said one inserted card.

10. A memory system, comprising:

(A) a plurality of encapsulated memory cards that individually include:

a programmable non-volatile memory and a controller of the memory,

a plurality of electrical contacts on an outer surface of the card, at least one of the contacts carrying data to and from the memory, only one of the contacts receiving commands to control operation of the controller and memory and sending a response, and a contact to receive a clock signal that operates the controller and memory, and

a plurality of registers that are programmable by command signals received through the command/response pin and readable by response signals sent through the command/status pin, including a programmable address register,

(B) a plurality of sockets which individually receive one of the plurality of cards, said sockets individually including:

at least a first pin positioned to connect with said at least one data contact of a card inserted therein, the first pins of the individual plurality of sockets being connected together into a common at least one data line,

a second pin positioned to connect with said only one command/response contact of a card inserted therein, the second pins of the individual sockets being connected into individual command/response lines,

a third pin positioned to connect with said clock signal contact of a card inserted therein, the third pins of the plurality of sockets being connected together into a common clock signal line, and

(C) a host device connected to send and receive data on said at least one common data line, to send a clock signal on the common clock signal line, and to normally simultaneously send operating commands to and receive response signals from an individual one of the cards over all of the individual command/response lines simultaneously by including an address of said individual card, except when distinct addresses in the address registers of the plurality of cards are being confirmed through one of the individual command/response lines at a time.

11. The memory system of claim 10, wherein said at least one common data line includes two or more data lines, the memory cards individually provide a response of the number of contacts that carry data to and from the card memory, this response of cards inserted into the plurality of sockets being readable by the host over the command/response lines, said host being connected to transfer data with the individual memory cards inserted in each of the plurality of sockets over one or more of the two or more data lines determined by the response numbers read by the host from the respective cards.

12. The memory system of claim 11, the clock signal on the common clock signal line has a frequency that remains the same without regard for

the number of the two or more data lines over which data are transferred with the individual memory cards.

13. A memory system, comprising:

a plurality of cards individually having a plurality of external contacts including at least one contact through which data are transferred into and out of a re-writeable non-volatile memory within the card, only one contact through which commands are received to operate the memory and response signals sent from the memory, and a contact to receive a clock signal to operate the memory,

a plurality of sockets into which said cards are individually insertable with their contacts electrically contacting a plurality of corresponding pins including at least one data pin, only one pin for command and response signals and a clock signal pin,

a host system having a single line carrying command and response signals that is selectively connectable by the host to the command and response signal pin of any one or all of the individual card sockets, said host system additionally having at least one line that is connected with said at least one data pin of each of the plurality of sockets to carry data to and from cards inserted therein, said host system also including a clock signal line connected with said clock signal pin of each of the plurality of sockets,

said plurality of cards individually including an address register into which an address of the card is confirmed to be unique by the host through the command and response line connected to a single card at a time through the command and response pin of the card socket in which the single card is inserted, and

said host sending additional commands to and receiving additional response signals from an individual one of the cards through said command and response line when connected to the command and response pins of all of the plurality of sockets by sending on the command and response line the address stored in the address register of said individual one of the cards.

14. A memory system, comprising:

a plurality of cards individually having a plurality of external contacts including one or more contacts through which data are transferred into and out of a re-writeable non-volatile memory within the card, a contact through which commands are received to operate the memory and response signals sent from the memory, and a contact to receive a clock signal to operate the memory,

a plurality of sockets into which said cards are individually insertable with their contacts electrically contacting a plurality of corresponding pins including two or more data pins, a pin for command and response signals and a pin for the clock signal,

a host system having a line carrying card command and response signals between it and the command and response pin of the plurality of sockets, a line carrying a clock signal of constant frequency over a line connected with said clock signal pin of each of the plurality of sockets, and two or more data carrying lines being connected with the two or more data pins of each of the plurality of sockets,

said plurality of cards individually having stored an indication of the number of contacts through which data are simultaneously transferrable, said stored indication being readable by the host over the command and response line, and

said host transferring data with the individual cards inserted into the plurality of sockets according to the indication stored in the individual cards.

15. The memory system of claim 14, wherein the host system includes a single line carrying command and response signals that is selectively connectable by the host to the command and response signal pin of any one or all of the individual card sockets, said plurality of cards individually including an address register into which an address of the card is confirmed to be unique by the host through the command and response line to a single card at a time when connected to the command and response pin of the card socket in which the single card is

inserted, and said host sending additional commands to and receiving additional response signals from an individual one of the cards through said command and response line when connected to the command and response pins of all of the plurality of sockets by sending on the command and response line the address stored in the address register of said individual one of the cards.

16. An encapsulated card including re-writeable non-volatile memory that has a plurality of contacts including a first group of one or more contacts through which data are simultaneously transferrable between the memory and an external host, a second group of one or more contacts receiving commands from an external host to operate the memory and sending signals to an external host of the status of the operation of the memory, third group of one or more contacts receiving a clock signal from which the memory operates, a register field that permanently stores an indication of the number of contacts within the first group, and an interface circuit connected to read data from and write data to the memory though the number of contacts of the first group according to the stored indication.

17. The card of claim 16, wherein the encapsulated card is 32 millimeters long, 24 millimeters wide and either 1.4 or 2.1 millimeters thick.

18. A plurality of cards, each according to claim 16, wherein the number of contacts in the first group and the corresponding stored indication include at least two different numbers.

19. The plurality of cards of claim 18, where in said at least two different numbers include one and four.

20. An encapsulated card including re-writeable non-volatile memory that has a plurality of contacts including a first group of one or more contacts through which data are simultaneously transferrable between the memory

and an external host, a second group of one or more contacts receiving commands from an external host to operate the memory and sending signals to an external host of the status of the operation of the memory, third group of one or more contacts receiving a clock signal from which the memory operates, a register field that stores an address of the card that is readable by the host through the first group of contacts, and a random number generator that writes the card address into said register field.

21. A method of transmitting a serial stream of data bits between first and second devices, comprising:

determining a first number of data lines between the first and second devices, from one to a plurality of lines, with which said devices can communicate data bits in parallel,

switching the data stream between said first number of lines at one of the first and second devices after each occurrence of a second number of one or more bits thereof having passed to another of said first and second devices, and

reassembling the serial data stream at said another of the first and second devices by switching between said first number of data lines after each occurrence of the second number of one or more bits having been received.

22. The method of claim 21, wherein said first number is stored in one of the first and second devices, and further wherein the stored first number is read by the other of said first and second devices.

23. The method of either of claims 21 or 22, wherein the second number is one data bit.